Lab Module 3: CMOS Inverter Switching Characteristics & Delay Analysis

Course: Digital VLSI Design / CMOS Circuit Design

Module Title: CMOS Inverter: Dynamic Performance, Delay Optimization, and Power Analysis

Duration: 3-4 Hours (inclusive of pre-lab preparation, simulation, and post-lab analysis)

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1. Lab Objectives

Upon successful completion of this laboratory module, students will be able to:

- **Perform Transient Simulations:** Accurately set up and execute transient simulations for a CMOS inverter to capture its dynamic input and output waveforms.
- **Measure Propagation Delays:** Precisely measure tpHL, tpLH, and tp from simulated waveforms using appropriate measurement techniques.
- **Analyze Impact of Load Capacitance:** Quantitatively demonstrate and explain the relationship between external load capacitance and the propagation delay of the inverter.
- **Investigate Transistor Sizing Effects:** Analyze how varying the W/L ratios of NMOS and PMOS transistors influences propagation delays and achieve balanced rise/fall times.
- **Differentiate Power Components:** Calculate and distinguish between dynamic and static power dissipation in a CMOS inverter under various operating conditions.
- **Design for Constraints:** Apply iterative design methodologies to size a CMOS inverter to meet specified propagation delay and initial power targets.

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2. Pre-Lab Preparation

Before coming to the lab session, ensure you have:

- **Reviewed Lecture Notes:** Revisit lecture material on CMOS inverter transient response, propagation delay definitions, and basic power dissipation concepts.
- **Understood Device Models:** Familiarize yourself with the basic SPICE parameters for NMOS and PMOS transistors (e.g., VT, Kn′, Kp′, λ, etc.).
- **Familiarized with EDA Tool:** Ensure you are comfortable with the basic functionalities of your chosen circuit simulator (e.g., creating schematics, selecting analysis types, using probes/cursors).
- **Simulated Basic Inverter:** (Optional but Recommended) Try to set up a simple CMOS inverter and run a transient simulation to get familiar with the process before the lab.

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3. Required Tools & Materials

- **Computer Workstation:** A PC or workstation with sufficient processing power and memory.
- **Circuit Simulator Software:**
    - **Commercial:** Cadence Virtuoso with Spectre, Synopsys Custom Compiler with HSpice, or similar.
    - **Open-Source/Freeware:** LTSpice, ngspice.
- **Technology Files/Models:** Access to a basic 0.18 µm or 0.25 µm CMOS technology model file (`.lib` or `.mod` file) for NMOS and PMOS transistors. Your instructor will provide this.
- **Spreadsheet Software:** Microsoft Excel, Google Sheets, or equivalent for data plotting and analysis.

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4. Lab Procedures & Experiments

Important Note: Throughout these procedures, save your schematics and simulation results frequently. Label your plots clearly for your lab report.

Experiment 1: Basic CMOS Inverter Transient Response

1. **Objective:** Observe the fundamental transient behavior of a CMOS inverter.
2. **Procedure:**
    - **Schematic Setup:**
        - Create a new schematic in your chosen simulator.
        - Instantiate one NMOS and one PMOS transistor.
        - Connect them to form a CMOS inverter: PMOS source to VDD, NMOS source to GND, gates connected for input, drains connected for output.
        - Connect VDD and GND global nets.
    - **Transistor Sizing (Initial):**
        - Set initial W/L ratios. For this experiment, use:
            - NMOS: W=0.5µm, L=0.18µm (or your technology's minimum length).
            - PMOS: W=1.0µm, L=0.18µm (to achieve a common initial PMOS/NMOS width ratio of 2 for balanced delays).
    - **Input Signal Definition:**
        - Add a voltage source at the input (e.g., a `VPULSE` source in SPICE).
        - Configure the pulse:
            - V1=0V (Low voltage)
            - V2=VDD (High voltage, use your technology's nominal VDD, e.g., 1.8V for 0.18 µm)
            - Tdelay=0s
            - Trise=1ns
            - Tfall=1ns
            - Tpulse=50ns (Pulse width)
            - Tperiod=100ns (Total period, ensures multiple cycles)

- **Load Definition:**
  - Add a **load capacitance** (C) of **50 fF (femtoFarads)** from the output node to GND. This represents the parasitic capacitance of interconnects and input capacitance of subsequent gates.
- **Simulation Setup:**
  - Select "Transient Analysis."
  - Set "Stop Time" to 200ns (to observe at least two full cycles).
  - Set "Maximum Timestep" to 0.1ns (or smaller for finer resolution).
- **Run Simulation:** Execute the simulation.
- **Waveform Analysis:**
  - Plot the input voltage and output voltage waveforms on the same graph.
  - **Capture a screenshot** of the input and output waveforms, clearly showing at least one complete switching cycle.

Experiment 2: Measurement of Propagation Delays

1. **Objective:** Accurately measure tpHL, tpLH, and tp from the simulated waveforms.
2. **Procedure:**
   - **Using Waveform Cursors:**
     - Navigate to your simulation results viewer.
     - Place two cursors on the **input waveform**. Identify the time point where the input crosses 50% of VDD (for both rising and falling edges).
     - Place two other cursors on the **output waveform**. Identify the corresponding time points where the output crosses 50% of VDD.
     - **For tpHL:** Measure the time difference between the 50% point of the input *rising* edge and the 50% point of the output *falling* edge.
     - **For tpLH:** Measure the time difference between the 50% point of the input *falling* edge and the 50% point of the output *rising* edge.
     - Calculate tp=(tpHL+tpLH)/2.
   - **Using Automated Measurement Functions (If Available):** Explore and utilize your simulator's built-in functions for delay measurement (e.g., `MEASURE TRAN` commands in SPICE, specific waveform calculator functions). This is generally more precise.
   - **Record Results:** Create a table in your lab notebook or a spreadsheet to record the measured values of tpHL, tpLH, and tp.

Experiment 3: Impact of Load Capacitance on Delay

1. **Objective:** Investigate how varying the load capacitance affects the inverter's propagation delay.
2. **Procedure:**
   - **Modify Existing Schematic:** Use the inverter schematic from Experiment 1.
   - **Parametric Sweep Setup:** Configure a parametric sweep for the load capacitance (`C_load`).

- **Sweep Values:** Vary C_load over a range (e.g., 10 fF, 20 fF, 50 fF, 100 fF, 200 fF, 500 fF, 1 pF).
- **Run Sweep:** Execute the transient simulation with the capacitance sweep.
- **Data Collection:** For each C_load value:
  - Measure tpHL, tpLH, and tp.
  - Record all measured values in a table.
- **Plotting:**
  - Create a graph plotting tp (Y-axis) against C_load (X-axis).
  - **Capture a screenshot** of this plot.
- **Analysis:** Observe and describe the relationship between tp and C_load.

Experiment 4: Impact of Transistor Sizing (W/L) on Delay

1. **Objective:** Analyze how adjusting the W/L ratios of NMOS and PMOS transistors influences propagation delays and how to achieve balanced delays.
2. **Procedure:**
   - **Reset Load:** Set C_load back to 50 fF (or a fixed reasonable value).
   - **Part A: Varying NMOS Width (W_N) while keeping PMOS fixed:**
     - Keep PMOS: W=1.0µm, L=0.18µm.
     - Vary NMOS WN: 0.25µm,0.5µm,1.0µm,2.0µm,4.0µm. Keep LN=0.18µm.
     - For each WN, measure tpHL, tpLH, and tp. Record in a table.
   - **Part B: Varying PMOS Width (W_P) while keeping NMOS fixed:**
     - Keep NMOS: W=0.5µm, L=0.18µm.
     - Vary PMOS WP: 0.5µm,1.0µm,2.0µm,4.0µm,8.0µm. Keep LP=0.18µm.
     - For each WP, measure tpHL, tpLH, and tp. Record in a table.
   - **Part C: Achieving Balanced Delays:**
     - Based on your findings from Part A and B, determine an optimal PMOS W/L to NMOS W/L ratio (β ratio) that results in tpHL≈tpLH.
     - Set the transistor sizes accordingly (e.g., if you found β≈2, set WN=0.5µm,WP=1.0µm).
     - Measure tpHL, tpLH, and tp for this "balanced" inverter.
   - **Plotting:**
     - Create plots showing tpHL, tpLH, and tp vs. NMOS Width (from Part A) and PMOS Width (from Part B).
     - **Capture screenshots** of these plots.
   - **Analysis:** Discuss the individual and combined effects of WN and WP on delays. Explain why a specific β ratio is often chosen.

Experiment 5: Introduction to Power Analysis

1. **Objective:** Measure and understand dynamic and static power dissipation in the CMOS inverter.
2. **Procedure:**
   - **Use Balanced Inverter:** Use the balanced inverter from Experiment 4, Part C, with C_load = 50 fF.

- **Part A: Dynamic Power Measurement:**
  - Set input `T_period` to 100ns (equivalent to fclock=10 MHz).
  - Run transient simulation.
  - **Measure Dynamic Power:**
    - In your simulator, plot the instantaneous power delivered by the VDD source ($P(t)=VDD \cdot IDD(t)$).
    - Use the average measurement function over several full cycles (e.g., from 50ns to 150ns to avoid initial transients) to find the average dynamic power.
    - Record this value.
  - **Verify with Formula:** Calculate $Pdynamic=\alpha CloadVDD2fclock$. Assume $\alpha=1$ (since the inverter switches every cycle). Compare with your measured value.
  - **Effect of Frequency:** Repeat the dynamic power measurement for `T_period = 200ns` (fclock=5 MHz) and `T_period = 50ns` (fclock=20 MHz). Record and discuss the trend.
- **Part B: Static Power Measurement:**
  - **Method 1 (DC Operating Point):**
    - Change the input voltage source to a DC voltage source, setting its value to 0V (logic LOW) and run a **DC operating point analysis**.
    - Measure the IDDQ (quiescent supply current) from the VDD source. Calculate $Pstatic=VDD \cdot IDDQ$.
    - Repeat for input voltage set to VDD (logic HIGH). You should observe very low current in both cases for an ideal CMOS inverter (some leakage will be present in real models).
  - **Method 2 (Long Transient):**
    - Set the input pulse to stay at 0V for a very long duration (e.g., Tpulse=500ns, Tperiod also very long).
    - Run a transient simulation for a duration where the output is stable (e.g., 500ns).
    - Measure the average supply current (IDD) from the VDD source during the stable period.
    - Calculate $Pstatic=VDD \cdot IDD$.
  - **Record Results:** Note down the static power measured by both methods.

Experiment 6: Designing an Inverter for Specific Delay Constraints

1. **Objective:** Apply iterative design principles to meet a target propagation delay.
2. **Procedure:**
   - **Design Specification:**
     - Your goal is to design an inverter with an **average propagation delay (tp) of approximately 25 ps** (picoseconds) while driving a **load capacitance of 100 fF**.
     - Use VDD from your technology model.

        - Maintain the PMOS/NMOS width ratio for balanced delays found in Experiment 4, Part C.
    - **Iterative Design Steps:**
        - **Initial Guess:** Start with the "balanced" inverter from Experiment 4.
        - **Simulate:** Run a transient simulation with the 100 fF load.
        - **Measure:** Determine the current tp.
        - **Adjust:**
            - If tp is too high (slower than 25 ps), incrementally increase *both* NMOS and PMOS widths (maintaining your chosen β ratio).
            - If tp is too low (faster than 25 ps) or you want to minimize area/power, incrementally decrease both widths.
        - **Repeat:** Continue simulating, measuring, and adjusting until you achieve a tp close to 25 ps (e.g., within +/- 5%).
    - **Record Final Design:**
        - Note down the final W/L ratios of your NMOS and PMOS transistors.
        - Record the final measured tpHL, tpLH, and tp.
    - **Waveform Capture:** Take a screenshot of the input and output waveforms for your final optimized design, highlighting the measured delay.
    - **Power Calculation:** Calculate the dynamic and static power dissipation for your final optimized inverter.

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5. Lab Report Guidelines

Your lab report should be a clear, concise, and professional document presenting your experiments, results, and analysis.

Report Structure:

1. **Title Page:**
    - Lab Module Title and Number
    - Your Name, Student ID
    - Course Name, Date of Submission
    - Instructor's Name
2. **1. Objectives:** (Copy directly from Lab Objectives section above).
3. **2. Pre-Lab Activities:** Briefly mention any specific pre-lab preparation you did.
4. **3. Tools Used:** List the specific simulator software (version if possible) and technology file used.
5. **4. Procedures and Results:**
    - For each Experiment (1 through 6):
        - Briefly state the **purpose** of the experiment.
        - Describe the **setup** (e.g., initial W/L, input pulse parameters, load capacitance).
        - Present **results** clearly:
            - **Screenshots** of relevant waveforms and plots (from Experiments 1, 3, 4, 6). Ensure plots are clearly labeled with axes and units.

        - **Tables** summarizing measured data (from Experiments 2, 3, 4, 5, 6).
    - **Analysis and Discussion:**
        - Explain what you observed in the waveforms and plots.
        - Discuss the relationships (e.g., tp vs. Cload, tp vs. W/L).
        - Explain *why* these relationships exist (e.g., increased load requires more charge, wider transistors provide more current).
        - Compare theoretical expectations with your simulation results.
        - For Experiment 4, explain how you achieved balanced delays and why it's important.
        - For Experiment 5, differentiate between dynamic and static power, discussing their dependencies.
        - For Experiment 6, explain your iterative design process and how you arrived at the final dimensions. State your final W/L values and the achieved delay and power.
6. **5. Conclusion:**
    - Summarize your key findings and what you learned from each experiment.
    - Reiterate whether you met the lab objectives.
    - Discuss any challenges encountered and how you resolved them.
    - Suggest potential improvements or future work related to these experiments.

Formatting and Style:

- Use clear headings and subheadings.
- All figures (plots, screenshots) and tables must be numbered and have descriptive captions.
- Refer to all figures and tables in your text.
- Use appropriate units for all measurements (e.g., ns, ps, fF, pF, µm, mW, µW).
- Ensure professional language and grammar.

This lab module structure provides a clear, step-by-step guide for students to conduct experiments, analyze results, and gain a deep understanding of CMOS inverter dynamic behavior and design.